

# Low current density, inverted polarity, high-speed, top-emitting 850 nm vertical-cavity surface-emitting lasers

A.N. Al-Omari and K.L. Lear

**Abstract:** High-speed, oxide-confined, inverted polarity ( $n$ -up), polyimide-planarised 850 nm vertical-cavity surface-emitting lasers (VCSELs) were fabricated and characterised. The lasers exhibit a  $-3$  dB frequency modulation bandwidth ( $f_{3\text{dB}}$ ) up to 15.2 GHz with a  $10\ \mu\text{m}$  oxide aperture diameter, at the lowest current density ( $J_{\text{bias}}$ ) ever reported of  $6.4\ \text{kA}/\text{cm}^2$ . The ratio  $f_{3\text{dB}}^2/J_{\text{bias}} = 36.1\ (\text{GHz}^2/\text{kA}/\text{cm}^2)$  represents a 21% increase when compared with the highest previously reported ratio. The threshold voltage and current were as low as 1.45 V and 0.9 mA, respectively, with a series resistance of  $65\ \Omega$ . A rate-equation-based thermal VCSEL model was used to predict the device performance at different temperatures. Good agreements between measured and simulated DC characteristics were obtained.

## 1 Introduction

Three approaches to greater local area network (LAN) link bandwidth are: parallel fibre ribbons, wave division multiplexing and faster single-channel modulation rates. Since the vertical-cavity surface-emitting lasers (VCSELs) are widely used in shortwave length ( $\sim 850\ \text{nm}$ ) LAN transmitters, it is important to develop high-speed reliable VCSELs for faster single-channel systems. The main factors affecting the VCSELs modulation response are the intrinsic (relaxation) oscillation frequency and parasitic circuit effects [1]. Very high relaxation oscillation frequencies of 58 and 70 GHz were reported using the damping factor parabolic dependence on the resonant frequency prior to saturation and an electrically pulsed VCSEL [2], respectively. Also, optical nonlinear gain limits the bandwidth of VCSELs by inhibiting high-resonance frequencies [1, 3].

Large values of extrinsic parasitic circuit elements can restrict the maximum modulation bandwidth, and thus prevent achieving the intrinsic frequency limits. The main extrinsic factors are parasitic circuit effects, multi-mode operation and junction heating. To increase the modulation rate, these extrinsic factors need to be addressed.

Many researchers have reported various methods for reducing the parasitic circuit effects, such as parasitic resistances and capacitances associated with VCSELs. Different approaches to reduce the VCSELs series resistances (top and bottom mirrors) and capacitances (junction, oxide and pad) were reported in [1, 4–7]. Another factor

that limits the maximum bandwidth of VCSELs is the number of transverse modes [8]. High-modulation bandwidth was obtained from devices that operate in a single mode for an extended range above the threshold [7]. Although there are many inter-related factors that contribute to a single-mode operation, such as current distribution, gain-mode overlap, spatial hole burning and loss of the higher order modes, one of the essential VCSEL fabrication issues that can promote a single-mode operation is the oxide aperture diameter, where the active diameter is small enough to allow only a single-mode operation. Keeping this in mind, and since the laser diode bandwidth varies as  $(J_{\text{bias}} - I_{\text{th}})^{1/2}$ , the laser must be biased at a current  $I_{\text{bias}}$  several times than the threshold current ( $I_{\text{th}}$ ) in order to reach high frequencies. As a result, the current density ( $J_{\text{bias}}$ ) at which these devices operate is very high given the small oxide aperture needed for single-mode operation, which in turn produces significant junction heating that would impact the device reliability [9–11]. Recently, researchers have reported other techniques, such as the use of a multi-oxide layer and a micro-machined surface relieved structure [12, 13] or the incorporation of a photonic crystal pattern with an oxide-confined VCSEL structure [14].

This paper presents work on high-speed, oxide-confined, inverted polarity, polyimide-planarised 850 nm VCSELs. The reported devices incorporate previously reported epitaxial mirror designs and  $p$ -type substrates for low-series resistances [15], as well as HD-8000 polyimide for planarisation and parasitic pad capacitance reduction [16]. The lasers exhibit a  $-3$  dB frequency modulation bandwidth up to 15.2 GHz with a  $10\ \mu\text{m}$  oxide aperture diameter at the density of only  $6.4\ \text{kA}/\text{cm}^2$ . A relatively large oxide aperture diameter results in a low current density which should improve reliability [9–11], and is discussed later. To our knowledge, the ratio of the frequency modulation bandwidth squared to the current density ( $f_{3\text{dB}}^2/J_{\text{bias}}$ ), which is  $36.1\ (\text{GHz}^2/\text{kA}/\text{cm}^2)$  in our case, is the highest ratio ever reported, and represents a 21% increase compared

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doi:10.1049/iet-opt:20070024

Paper first received 22nd March and in revised form 31st May 2007

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**Table 1: Active area sizes, differential efficiencies, current densities and –3 dB modulation bandwidths data from other researchers' publications including the results reported in this paper**

References	Aperture size ( $\mu\text{m}^2$ )	Slope efficiency (W/A)	$J_{\text{bias}}$ ( $\text{kA}/\text{cm}^2$ ) <sup>a</sup>	$f_{3\text{dB}}$ (GHz)	$f_{3\text{dB}}^2/J_{\text{bias}}$ ( $\text{kA}/\text{cm}^2$ )	$J_{\text{bias}}$ ( $\text{kA}/\text{cm}^2$ )/10 ( $\text{kA}/\text{cm}^2$ ) <sup>b</sup>
[28]	$\pi 3.0^2$	0.71	46	15	4.9	4.6
[29]	$3 \times 3$	0.58	50	16.3	5.3	5.0
[30]	$\pi 3.5^2$	0.32	24.7	11	4.9	2.5
[31]	$\pi 4.0^2$	0.10	28.3	14	6.9	2.8
[32]	$\pi 1.6^2$	0.55	27.8	15.2	8.3	2.8
[33]	$\pi 3.25^2$	0.68	30.1	19	12.0	3.0
[34]	$\pi 5.0^2$	0.25	10.4	14.5	20.1	1.0
[7]	$4 \times 4$	0.58	30	20	13.3	3.0
[1]	$6 \times 6$	0.29	10.4	7	4.7	1.0
[14]	$6 \times 6$	0.25	12	9	6.8	1.2
[20] <sup>c</sup>	$\pi 4.5^2$	0.44	10.5	9.8	9.1	1.1
[35]	$\pi 3.0^2$	0.33	18.2	20	22.0	1.8
[16] <sup>c</sup>	$\pi 3.5^2$	0.10	11.7	17	24.7	1.2
[36] <sup>c</sup>	$\pi 5^2$	0.16	8.9	16.3	29.9	0.9
Present work	$\pi 5^2$	0.09	6.4	15.2	36.1	0.6

<sup>a</sup>  $J_{\text{bias}}$  was calculated based on the reported active area size and does not count for the current spreading

<sup>b</sup> Industrial current density benchmark for reliability  $\leq 10 \text{ kA}/\text{cm}^2$

<sup>c</sup> Previous work reported by author and collaborators

with the highest previously published and reported ratio results, which is revealed in Table 1.

## 2 Epitaxial structure and device fabrication

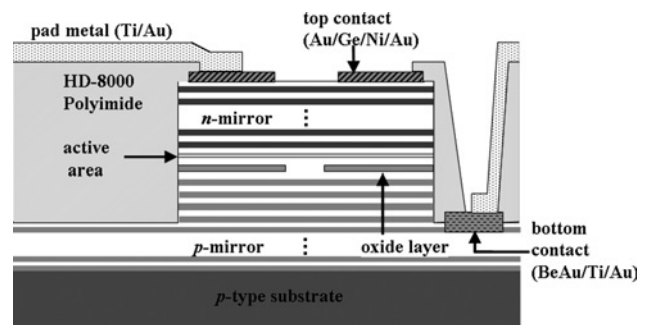
Top-emitting, high-speed 850 nm VCSELs were fabricated from an AlGaAs structure on a *p*-type substrate [15] grown by metal–organic chemical vapour deposition. Accordingly, the *n*-side-up VCSELs are electrically compatible with *npn* bipolar-junction transistors used in the driver circuitry for VCSEL arrays. The active region consists of four GaAs quantum wells with  $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$  barriers. The *n*-mirror above the active region is a 25-period, Si-doped  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  (high Al content)/ $\text{Al}_y\text{Ga}_{1-y}\text{As}$  (low Al content) distributed Bragg reflector (DBR). The C-doped, 35-period *p*-mirror below the active region also employs  $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{Al}_y\text{Ga}_{1-y}\text{As}$  DBRs except for a single low-index quarter wavelength layer adjacent to the cavity with  $\text{Al}_{0.98}\text{Ga}_{0.02}\text{As}$  composition. The *n*-DBR was terminated with a phase-matching heavily doped ( $n^{++}$ -GaAs) contact layer.

A processing sequence using five photomasks (mesa, top-contact, bottom-contact, planarisation, interconnects) was used to fabricate oxide-confined, polyimide-planarised VCSELs with coplanar waveguide (GSG) probe pads. Device fabrication began with the formation of cylindrical mesas by etching the surrounding semiconductor to a depth of  $5 \mu\text{m}$  in the *p*-type bottom mirror using a load-locked chemically assisted ion beam etching system.

Wet-oxidation was used to provide current confinement and lateral index guiding to the lasing mode. The sample was oxidised using a Lindberg tube furnace in a  $440^\circ\text{C}$  steam environment for 10 min [9]. The oxidation rate was about  $1.0 \mu\text{m}/\text{min}$  for the  $\text{Al}_{0.98}\text{Ga}_{0.02}\text{As}$  layer resulting in an active area diameter of  $10 \mu\text{m}$  for devices with a mesa diameter of  $30 \mu\text{m}$ . To form the annular *n*-type contact on top of the mesa, Au/Ge/Ni/Au with a total thickness of  $\sim 1400 \text{ \AA}$  were evaporated in sequence using the E-beam evaporator. The Ni layer was added as a wetting agent while the last Au layer was added to protect

the Ni layer from oxidation. Before the deposition at the bottom *p*-type contact, the sample was soaked for about 15 s in an HCl/H<sub>2</sub>O (1:1) solution to remove the high Al content layer surface or the oxide layer formed at the low Al content layer surface during the oxidation process. This step reduces the bottom contact ohmic contact resistance. BeAu(pre-alloyed with 1% Be by weight)/Ti/Au with a total thickness of  $\sim 1600 \text{ \AA}$  were evaporated onto the partly etched *p*-DBR bottom mirror to form the *p*-type bottom contact, which is connected to the substrate. Contacts were alloyed for 30 s at  $420^\circ\text{C}$  in nitrogen ambient.

After contact formation, HD-8000 positive tone photo-sensitive polyimide was spun on the sample for field insulation and device planarisation. The central portion of the mesa top as well as the lower *p*-type contact were exposed and developed prior to curing the polyimide at  $350^\circ\text{C}$  for 30 min in nitrogen ambient. Polyimide planarisation offers lower metal interconnect and pad capacitance than conventional oxide or nitride passivation since it has a relatively low dielectric constant ( $\epsilon_r = 3.4$ ), and can readily produce thick layers, about  $5.0 \mu\text{m}$  of cured polyimide in this case. A ground-signal-ground (GSG) contact configuration with a  $125 \mu\text{m}$  pitch size of Ti/Au with a



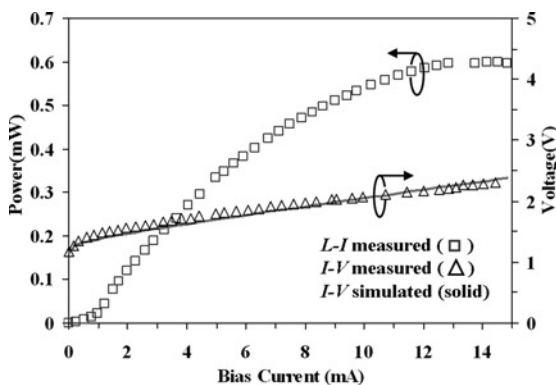
**Fig. 1** Schematic cross-section of an oxide-confined high-speed VCSEL ready for testing

total thickness of about 3300 Å was deposited for metal interconnects and coplanar waveguide probe pads. Fig. 1 shows a schematic cross-section of an oxide-confined high-speed VCSEL that was fabricated using the above described process ready for testing.

### 3 Results and discussion

DC characteristics of completed VCSELs were measured at room temperature using a probe station, an HP 4145A semiconductor parameter analyser and a silicon photodiode with  $10 \times 10 \text{ mm}^2$  active area and  $\sim 0.6 \text{ A/W}$  responsivity at  $\lambda \sim 850 \text{ nm}$ . Fig. 2 shows the continuous-wave (CW) light output against current ( $L-I$ ) and voltage against current ( $I-V$ ) characteristics of a VCSEL with a  $30 \mu\text{m}$  mesa diameter and  $10 \mu\text{m}$  oxide-confined aperture diameter. The threshold voltage and current were as low as  $1.5 \text{ V}$  and  $0.9 \text{ mA}$ , respectively, with a series resistance of  $65 \Omega$  and a peak differential efficiency of  $\sim 0.09 \text{ W/A}$ . The low slope efficiency is due to the large number of top DBR periods. The expression  $V_F(I_F) = R_s I_F + [\ln(I_F/I_{\text{sat}}) m k_B T] / q$  [14] was used to obtain the expected  $I-V$  characteristic, where  $V_F$  and  $I_F$  are the forward bias current and voltage,  $I_{\text{sat}}$  is the saturation current,  $R_s$  is the total series resistance,  $T$  is the temperature ( $300 \text{ K}$ ),  $k_B$  is the Boltzmann's constant ( $1.38 \times 10^{-23} \text{ J/K}$ ),  $q$  is the electron charge  $1.6 \times 10^{-19} \text{ C}$  and  $m$  is the diode ideality factor. The  $I_{\text{sat}}$  value used was  $\sim 6 \times 10^{-16} \text{ mA}$  [17]. For best fit,  $m$  and  $R_s$  values were determined to be  $1.4$  and  $65 \Omega$ , respectively. Fig. 2 shows a comparison of the calculated and experimental  $I-V$  characteristics of a  $10 \mu\text{m}$  active diameter VCSEL under test.

The thermal resistance of VCSEL ( $R_{\text{th}}$ ) was determined by measuring the wavelength dependence of the laser spectra as a function of the dissipated electrical input power ( $P_d$ ), which is fitted along a straight line with a slope of  $(\delta\lambda/\delta P_d)$  [18, 19]. Using a typical value for mode shift ( $\delta\lambda/\delta T \sim 0.07 \text{ nm/K}$ ) in GaAs-based VCSELs [18, 19], VCSEL thermal resistance ( $R_{\text{th}}$ ) was obtained,  $R_{\text{th}} = [(\delta\lambda/\delta P_d)/0.07 \text{ nm/K}]$ . VCSELs with an active diameter of  $10 \mu\text{m}$  exhibited  $R_{\text{th}}$  of  $2.65^\circ\text{C/mW}$ . The  $R_{\text{th}}$  approximately followed the analytical estimation  $R_{\text{th}} = 1/(2\xi a)$  [18], for heat spreading from a uniform temperature disc on a homogenous, isotropic, semi-infinite substrate, where  $a$  is the active diameter and  $\xi$  is the substrate thermal conductivity. To investigate the effect of the DBR alloy scattering,  $R_{\text{th-cal}}$  was calculated with  $R_{\text{th-cal}} = 1/(2\xi a)$  for the  $10 \mu\text{m}$  active diameter device. For a best fit to the measured value of  $R_{\text{th}} = 2.65^\circ\text{C/mW}$ , we obtained  $\xi = 0.37 \text{ W/cm K}$ . As expected, the DBR alloy scattering



**Fig. 2** CW  $L-I-V$  characteristics measured (data points) and simulated (solid line) for a  $30 \mu\text{m}$  mesa diameter VCSEL with a  $10 \mu\text{m}$  active diameter

reduces  $\xi$  [18] compared to GaAs ( $\xi = 0.45 \text{ W/cm K}$ ) and AlAs ( $0.9 \text{ W/cm K}$ ). The reported  $R_{\text{th}}$  value for the present device is higher than some of the values reported by others [19, 20]. This is attributed to the fact that the devices reported in [19, 20] have plated metal heatsinks of  $8.5 \mu\text{m}$  Au ( $\xi \sim 3.2 \text{ W/cm K}$ ) and  $2 \mu\text{m}$  of Cu ( $\xi \sim 4.0 \text{ W/cm K}$ ), respectively, with a thin  $\text{Si}_3\text{N}_4$  ( $\xi \sim 0.08\text{--}0.3 \text{ W/cm K}$ ) layer deposited underneath to insulate electrically the mesa sidewalls from the plated heatsinks. In this context, the present devices have no heatsinking mechanism because of using polyimide with a very low thermal conductivity of  $0.002 \text{ W/cm K}$  [21]. It is believed that using the same plated heatsink approach reported in [19, 20] would reduce  $R_{\text{th}}$ , even though this approach can increase parasitic capacitance. However, using diamond rather than  $\text{Si}_3\text{N}_4$  for mesa sidewall isolation before plating could somewhat reduce thermal resistance due to diamonds very high thermal conductivity ( $\xi \sim 15\text{--}20 \text{ W/cm K}$ ) [22], as well as parasitic capacitance due to diamonds low relative dielectric constant ( $\epsilon_r \sim 5.6$ ) compared to that of  $\text{Si}_3\text{N}_4$  ( $\epsilon_r \sim 7.6$ ).

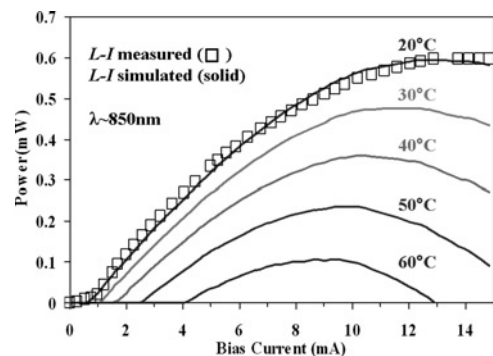
At the time of the device testing, the probe station available was equipped with a constant temperature stage rather than a temperature controlled one. Therefore a rate-equation-based thermal VCSEL model [23] was used to predict the device  $L-I$  performance at different temperatures. The VCSELs model with  $L-I$  characteristics above the threshold can be modelled using [23].

$$P_o = \eta(I - I_{\text{tho}} - I_{\text{off}}(T)) \quad (1)$$

where  $P_o$  is the optical output power,  $I$  is the injection current,  $\eta$  is the differential slope efficiency where its temperature dependence is assumed to have a negligible impact on the output power [24],  $I_{\text{tho}}$  is the threshold current and  $I_{\text{off}}(T)$  is an empirical thermal offset current which is modelled in [23] using a fourth order polynomial function of the VCSEL temperature  $T$ . Finally, the VCSEL temperature  $T$  is given by the expression reported in [23] using the approach detailed in [25, 26]. Substituting these expressions for  $I_{\text{off}}(T)$  and  $T$  [23, 25, 26] in (1) we obtain

$$P_o = \eta \left( I - I_{\text{tho}} - \left( \begin{array}{l} a_0 + a_1(T_o + (IV - P_o)R_{\text{th\_model}}) \\ + a_2(T_o + (IV - P_o)R_{\text{th\_model}})^2 \\ + a_3(T_o + (IV - P_o)R_{\text{th\_model}})^3 \\ + a_4(T_o + (IV - P_o)R_{\text{th\_model}})^4 \end{array} \right) \right) \quad (2)$$

where  $a_0$  through  $a_4$  is determined during the parameter extraction,  $R_{\text{th\_model}}$  is the VCSEL thermal impedance,  $T_o$



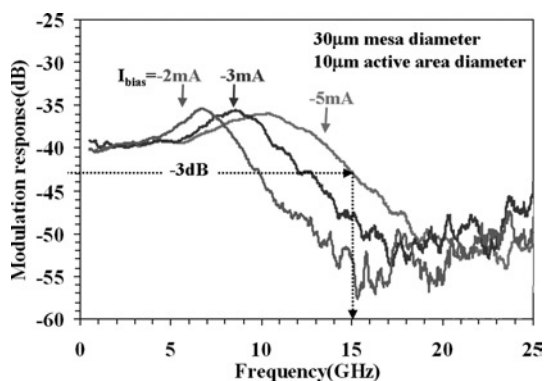
**Fig. 3** CW  $L-I$  characteristics measured (data points) and simulated (solid lines) for a  $30 \mu\text{m}$  mesa diameter VCSEL with a  $10 \mu\text{m}$  of oxide aperture diameter

is the ambient temperature [27] and  $V$  and  $I$  are the laser voltage and current, respectively.

To use the thermal VCSEL model, parameter extraction from measured data must be carried out. Using the experimental  $L-I$  data (squares) shown in Fig. 3, (2) can be optimised to obtain values for  $\eta$ ,  $R_{th\_model}$  and  $a_0$  through  $a_4$  which will reproduce the experimental  $L-I$ . Equation (2) best fits the measured data as shown in Fig. 3 using the following model parameters:  $a_0 = -4.5$  mA,  $a_1 = 6 \times 10^{-3}$  mA/K,  $a_2 = 6.4 \times 10^{-4}$  mA/K<sup>2</sup>,  $a_3 = 2.0 \times 10^{-8}$  mA/K<sup>3</sup>,  $a_4 = 3.0 \times 10^{-9}$  mA/K<sup>4</sup>,  $\eta = 0.09$ ,  $T_0 = 20^\circ\text{C}$  and  $R_{th\_model} = 2.75^\circ\text{C/mW}$ . Fig. 3 presents the measured  $L-I$  data at  $T_0 = 20^\circ\text{C}$  and the simulated  $L-I$  curves at 20, 30, 40, 50 and  $60^\circ\text{C}$  using (2). As illustrated in Fig. 3, the simulation results generated with these parameters at  $T_0 = 20^\circ\text{C}$  are in excellent agreement with experimental results. Fig. 3 also shows the simulated  $L-I$  characteristics for a  $30\ \mu\text{m}$  mesa diameter VCSEL with a  $10\ \mu\text{m}$  oxide aperture diameter at different temperatures. Both measured and simulated results in Fig. 3 showed that the maximum output optical power at  $20^\circ\text{C}$  was  $0.6$  mW. At higher temperatures, simulation results showed that the VCSELs output optical power is a rapid function of temperature. Thus, the maximum output power at CW operation is strongly dependent on temperatures and limited by the device thermal impedance.

The AC response measurement apparatus consisted of a probe station equipped with a  $20^\circ\text{C}$  constant temperature stage and Cascade Microtech air co-planar probes (ACP40),  $\sim 2$  m of multimode fibre, a NIST-calibrated, high-speed New Focus photodiode and attached New Focus amplifier, an HP 4145 semiconductor parameter analyser and an HP8510B vector network analyser (VNA). To obtain maximum DC optical power, the bare end fibre was actively aligned above the device under test using an  $x-y-z$ -theta positioning stage. The laser's modulation response ( $S_{21}$ ) was measured at various bias currents over a frequency range of up to  $26.5$  GHz. Fig. 4 shows the frequency modulation response of a VCSEL with a  $30\ \mu\text{m}$  mesa diameter and a  $10\ \mu\text{m}$  active area diameter where only results at three different bias currents are shown to maintain figure clarity.

As shown in Fig. 4, the  $10\ \mu\text{m}$  diameter aperture laser exhibits a modulation response of up to  $15.2$  GHz bandwidth when biased at  $I_{bias} = -5.0$  mA at room temperature. For lower-bias currents, the device exhibits modulation frequencies smaller than  $15.2$  GHz. Bias currents of  $-2$  and  $-3$  mA yielded  $-3$  dB bandwidths of  $9.9$  and  $12.2$  GHz, respectively. The modulation curves in Fig. 4 also reveal that the resonance peaks flattened and broadened with the



**Fig. 4** Frequency modulation response ( $S_{21}$ ) for a  $30\ \mu\text{m}$  mesa diameter VCSEL with a  $10\ \mu\text{m}$  active diameter at the DC biases indicated

increasing DC bias current. It is believed that this is due to the increase in damping phenomenon [18]. Based on the industrial current density benchmark for reliability, which is  $10\ \text{kA/cm}^2$  or less for VCSELs, the low-bias current density, such as  $6.4\ \text{kA/cm}^2$  necessary for the  $15.2$  GHz bandwidth in the  $10\ \mu\text{m}$  diameter device, should improve device reliability [9–11] and make it one step closer to commercialisation because higher current densities increase the internal temperature of the devices and could accelerate device degradation independent of junction temperature. A relatively low resistance [15] and very low pad and junction capacitances of  $65$  and  $135$  fF, respectively, insured that the device is not partially limited by electrical parasitics. Furthermore, a highly reflecting top 25-DBR mirror pairs explains the low current density due to the high internal photon density in the cavity.

Table 1 lists the active area sizes, differential efficiencies, current densities and  $-3$  dB modulation bandwidths data from the other published results in the literature. Comparison of our results with the previously published data for different device sizes and speeds is shown in Table 1 along with the representation of ratio of bandwidth squared to the bias current density,  $f_{3dB}^2/J_{bias}$  ( $\text{GHz}^2/\text{kA/cm}^2$ ). Since  $f_{3dB} = \text{MCEF}(I_{bias} - I_{th})^{1/2}$  and  $I_{bias} \gg I_{th}$  for high bandwidths,  $f_{3dB}^2/J_{bias} \simeq A \times \text{MCEF}^2$  where  $A$  is the active region area of the laser. Using  $f_{3dB}^2/J_{bias}$  effectively accounts for changes in MCEF of the laser with the active area becoming smaller for the current scales accordingly. The ratio  $f_{3dB}^2/J_{bias}$  is employed here to emphasise that the device presented in this paper demonstrates a high bandwidth while still not being too high for the current density. To our knowledge, the ratio  $f_{3dB}^2/J_{bias} = 36.1$  ( $\text{GHz}^2/\text{kA/cm}^2$ ) reported in this paper is the highest ratio ever reported and represents a 21% increase compared with the highest previously reported ratio [36]. Table 1 also shows the ratio of the reported current densities to the industrial current density benchmark mentioned earlier, where devices with  $J_{bias}/10\ \text{kA/cm}^2 \leq 1.0$  are considered reliable from an industrial point of view and for closer commercial production.

## 4 Conclusions

We have fabricated and characterised high-speed oxide-confined VCSELs that demonstrate excellent performance. The modulation bandwidth of VCSELs with typical size pads is as high as  $15.2$  GHz at a record low current density of  $6.4\ \text{kA/cm}^2$ . The rate-equation-based thermal VCSEL model resulted in a best fit to the measured data, and was used to predict the devices' performance at different temperatures. As the reported devices are multimode, future incorporation of techniques reported in [12–14] to suppress the higher order transverse modes and in [19, 20, 36] to reduce the thermal resistance should increase both the output power and the maximum  $-3$  dB frequency further.

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